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EXAMINER	
CHU, CHRIS C	

ART UNIT	PAPER NUMBER
2815	

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Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary	Application No.	Applicant(s)	
	10/042,812	CHIANG, CHENG-LIEN	
	Examiner	Art Unit	
	Chris C. Chu	2815	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If the period for reply specified above is less than thirty (30) days, a reply within the statutory minimum of thirty (30) days will be considered timely.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133).
- Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☐ Responsive to communication(s) filed on _____ .

2a)☐ This action is **FINAL**. 2b)☒ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1 - 60* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *1 - 60* is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☒ The drawing(s) filed on *09 January 2002* is/are: a)☐ accepted or b)☒ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

11)☐ The proposed drawing correction filed on _____ is: a)☐ approved b)☐ disapproved by the Examiner.

If approved, corrected drawings are required in reply to this Office action.

12)☐ The oath or declaration is objected to by the Examiner.

Priority under 35 U.S.C. §§ 119 and 120

13)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____ .

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

14)☐ Acknowledgment is made of a claim for domestic priority under 35 U.S.C. § 119(e) (to a provisional application).

a) ☐ The translation of the foreign language provisional application has been received.

15)☐ Acknowledgment is made of a claim for domestic priority under 35 U.S.C. §§ 120 and/or 121.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☒ Information Disclosure Statement(s) (PTO-1449) Paper No(s) 2 .
4) ☐ Interview Summary (PTO-413) Paper No(s). _____ .
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other: .

DETAILED ACTION

Drawings

1. The drawings are objected to under 37 CFR 1.83(a). The drawings must show every feature of the invention specified in the claims. Therefore, the limitation in claims 7, 17, 28, 47 and 57 "the terminal is within a periphery of a chip, and the lead is outside the periphery of the chip" must be shown or the feature(s) canceled from the claim(s). No new matter should be entered.

A proposed drawing correction or corrected drawings are required in reply to the Office action to avoid abandonment of the application. The objection to the drawings will not be held in abeyance.

2. Applicant is required to submit a proposed drawing correction in reply to this Office action. However, formal correction of the noted defect may be deferred until after the examiner has considered the proposed drawing correction. Failure to timely submit the proposed drawing correction will result in the abandonment of the application.

Claim Rejections - 35 USC § 112

3. The following is a quotation of the first paragraph of 35 U.S.C. 112:

> The specification shall contain a written description of the invention, and of the manner and process of making and using it, in such full, clear, concise, and exact terms as to enable any person skilled in the art to which it

pertains, or with which it is most nearly connected, to make and use the same and shall set forth the best mode contemplated by the inventor of carrying out his invention.

4. Claims 7, 17, 28, 47 are 57 rejected under 35 U.S.C. 112, first paragraph, as containing subject matter which was not described in the specification in such a way as to enable one skilled in the art to which it pertains, or with which it is most nearly connected, to make and/or use the invention. In claims 7, 17, 28, 47 and 57, the specification fails to disclose a terminal being within a periphery of a chip, a lead being outside the periphery of the chip and the lead being electrically connected to a pad without using wire bonds, TAB leads or solder joints. Specifically, it cannot be determined how the lead is electrically connected to the pad. Therefore, the limitation "the lead is outside the periphery of the chip" must be defined in the specification or the phrase cancelled from the claims. No new matter should be entered.

Claim Rejections - 35 USC § 102

5. The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action:

A person shall be entitled to a patent unless –

(b) the invention was patented or described in a printed publication in this or a foreign country or in public use or on sale in this country, more than one year prior to the date of application for patent in the United States.

6. Claims 1, 5 ~ 11 and 17 ~ 20 are rejected under 35 U.S.C. 102(b) as being anticipated by Shin et al.

Regarding claim 1, Shin et al. discloses in Fig. 1A, Fig. 1B, Fig. 10B and column 6, lines 36 ~ 40 a semiconductor package device, comprising:

- an insulative housing (40) with a top surface, a bottom surface, and a peripheral side surface between the top and bottom surfaces;
- a semiconductor chip (20) within the insulative housing, wherein the chip includes an upper surface and a lower surface, and the upper surface includes a conductive pad (31);
- a terminal (4 and 4') that protrudes downwardly from and extends through the bottom surface and is electrically connected to the pad; and
- a lead (2) that protrudes laterally from and extends through the side surface and is electrically connected to the pad,
- wherein the terminal and the lead are spaced and separated from one another outside the insulative housing, and the terminal and the lead are electrically connected to one another inside the insulative housing and outside the chip.

Regarding claim 5, Shin et al. discloses in Fig. 1A, Fig. 1B, Fig. 10B and column 6, lines 36 ~ 40 the terminal being the only electrical conductor that extends through the top or bottom surfaces and being electrically connected to the pad.

Regarding claim 6, Shin et al. discloses in Fig. 1A, Fig. 1B, Fig. 10B and column 6, lines 36 ~ 40 the terminal being a plated metal. Further, the limitation "plated metal" is a product-by-process claim language. Even though product-by-process claim is limited by and defined by the process, determination of patentability is based upon the product itself. The patentability of a product does not depend on its method of production. If the product in product-by-process claim is the same as or obvious from a product of the prior art, the claim is unpatentable even though the prior product is made by a different process. In re Thorpe, 227 USPQ 964, 966 (Fed. Cir.

1985) (citations omitted). A "product by process" claim is directed to the product per se, no matter how actually made, In re Hirao, **190 USPQ 15 at 17** (footnote 3). See also In re Brown, **173 USPQ 685**: In re Luck, **177 USPQ 523**; In re Fessmann, **180 USPQ 324**: In re Avery, **186 USPQ 116**; In re Wertheim, **191 USPQ 90 (209 USPQ 254** does not deal with this issue); and In re Marosi et al., **218 USPQ 289** final product per se which must be determined in a "product by, all of" claim, and not the patentability of the process, and that an old or obvious product, whether claimed in "product by process" claims or not. Note that Applicant has the burden of proof in such cases, as the above caselaw makes clear.

Regarding claims 7 and 17, Shin et al. discloses in Fig. 1A, Fig. 1B and Fig. 10B the terminal being within a periphery of the chip, and the lead being outside the periphery of the chip.

Regarding claim 8, Shin et al. discloses in Fig. 1A, Fig. 1B and Fig. 10B the device being devoid of an electrical conductor that extends through the top surface and being electrically connected to the pad.

Regarding claims 9 and 19, Shin et al. discloses in Fig. 1A, Fig. 10B and Fig. 14 the device including a plurality of terminals and leads, the chip including a plurality of pads, each of the terminals are electrically connected to one of the leads and one of the pads inside the insulative housing and outside the chip, the terminals are arranged as an array that protrudes downwardly from and extends through the bottom surface, and the leads are arranged as TSOP leads that protrude laterally from and extend through the side surface and an opposing peripheral side surface of the insulative housing.

Regarding claims 10 and 20, Shin et al. discloses in Fig. 1A, Fig. 1B and Fig. 10B the device being devoid of wire bonds, TAB leads and solder joints.

Regarding claim 11, Shin et al. discloses in Fig. 1A, Fig. 1B, Fig. 10B and column 6, lines 36 ~ 40 a semiconductor package device, comprising:

- an insulative housing (40) with a top surface, a bottom surface, and a peripheral side surface between the top and bottom surfaces;
- a semiconductor chip (20) within and surrounded by the insulative housing, wherein the chip includes an upper surface and a lower surface, the upper surface includes a conductive pad (31), the upper surfaces faces towards the bottom surface and faces away from the top surface, and the insulative housing contacts the lower surface;
- a terminal (4 and 4') that protrudes downwardly from and extends through the bottom surface and is spaced from the side surface and is electrically connected to the pad; and
- a lead (2) that protrudes laterally from and extends through the side surface and is electrically connected to the pad,
- wherein the terminal and the lead are spaced and separated from one another outside the insulative housing, and the terminal and the lead are electrically connected to one another inside the insulative housing and outside the chip.

Regarding claim 18, Shin et al. discloses in Fig. 10B and column 21, lines 22 ~ 28 the terminal being integral with a routing line that is plated on the lead inside the insulative housing, outside a periphery of the terminal and outside a periphery of the chip.

Claim Rejections - 35 USC § 103

7. The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

8. Claims 2 ~ 4, 12 ~ 16 and 21 ~ 40 are rejected under 35 U.S.C. 103(a) as being unpatentable over Shin et al. in view of Nakamura et al.

Regarding claim 2, Shin et al. discloses the claimed invention except for the insulative housing including a first single-piece housing portion that contacts the lead and is spaced from the terminal and a second single-piece housing portion that contacts the first single-piece housing portion and the terminal. However, Nakamura et al. discloses in Fig. 1 an insulative housing (7 and 8) including a first single-piece housing portion (7) that contacts the lead (2) and is spaced from the terminal (4) and a second single-piece housing portion (8) that contacts the first single-piece housing portion and the terminal. Thus, it would have been obvious to one of ordinary skill in the art at the time when the invention was made to modify Shin et al. by using the first and second single-piece housing portion for the insulative housing as taught by Nakamura et al. The ordinary artisan would have been motivated to modify Shin et al. in the manner described above for at least the purpose of providing a firm electrical connection with a circuit conductor layer formed on a substrate in a semiconductor device (column 5, lines 55 ~ 57).

Regarding claim 3, Nakamura et al. discloses in Fig. 1 and Fig. 4 the first single-piece housing portion contacting the lower surface.

Regarding claim 4, Nakamura et al. discloses in Fig. 1 the insulative housing consisting of the first and second single-piece housing portions.

Regarding claim 12, Shin et al. discloses the claimed invention except for the insulative housing consists of a first single-piece housing portion that contacts the lower surface and the lead and is spaced from the terminal and a second single-piece housing portion that contacts the first single-piece housing portion and the terminal. However, Nakamura et al. discloses in Fig. 1 an insulative housing (7 and 8) consists of a first single-piece housing portion (7) that contacts the lower surface and the lead (2) and is spaced from the terminal (4) and a second single-piece housing portion (8) that contacts the first single-piece housing portion and the terminal. Thus, it would have been obvious to one of ordinary skill in the art at the time when the invention was made to modify Shin et al. by using the first and second single-piece housing portion for the insulative housing as taught by Nakamura et al. The ordinary artisan would have been motivated to modify Shin et al. in the manner described above for at least the purpose of providing a firm electrical connection with a circuit conductor layer formed on a substrate in a semiconductor device (column 5, lines 55 ~ 57).

Regarding claim 13, Nakamura et al. discloses in Fig. 1 and Fig. 4 the first single-piece housing portion providing the top surface, the side surface and a peripheral portion of the bottom surface, and the second single-piece housing portion providing a central portion of the bottom surface within the peripheral portion of the bottom surface.

Regarding claim 14, Shin et al. discloses in Fig. 1A, Fig. 1B and Fig. 10B the peripheral portion of the bottom surface being outside a periphery of the chip, and the central portion of the bottom surface being within and outside the periphery of the chip.

Regarding claim 15, Nakamura et al. discloses in Fig. 1, column 6, lines 49 ~ 55 and column 8, lines 53 ~ 58 the first single-piece housing portion being a transfer molded material, and the second single-piece housing portion being not a transfer molded material. Further, the limitation "transfer molded material" is a product-by-process claim language. Even though product-by-process claim is limited by and defined by the process, determination of patentability is based upon the product itself. The patentability of a product does not depend on its method of production. If the product in product-by-process claim is the same as or obvious from a product of the prior art, the claim is unpatentable even though the prior product is made by a different process. In re Thorpe, 227 USPQ 964, 966 (Fed. Cir. 1985) (citations omitted). A "product by process" claim is directed to the product per se, no matter how actually made, In re Hirao, **190 USPQ 15 at 17** (footnote 3). See also In re Brown, **173 USPQ 685**: In re Luck, **177 USPQ 523**; In re Fessmann, **180 USPQ 324**: In re Avery, **186 USPQ 116**; In re Wertheim, **191 USPQ 90 (209 USPQ 254** does not deal with this issue); and In re Marosi et al., **218 USPQ 289** final product per se which must be determined in a "product by, all of" claim, and not the patentability of the process, and that an old or obvious product, whether claimed in "product by process" claims or not. Note that Applicant has the burden of proof in such cases, as the above caselaw makes clear.

Regarding claim 16, Nakamura et al. discloses in Fig. 1 the second single-piece housing portion including first and second opposing surfaces, the first surface contacting the lead and the second surface providing a portion of the bottom surface.

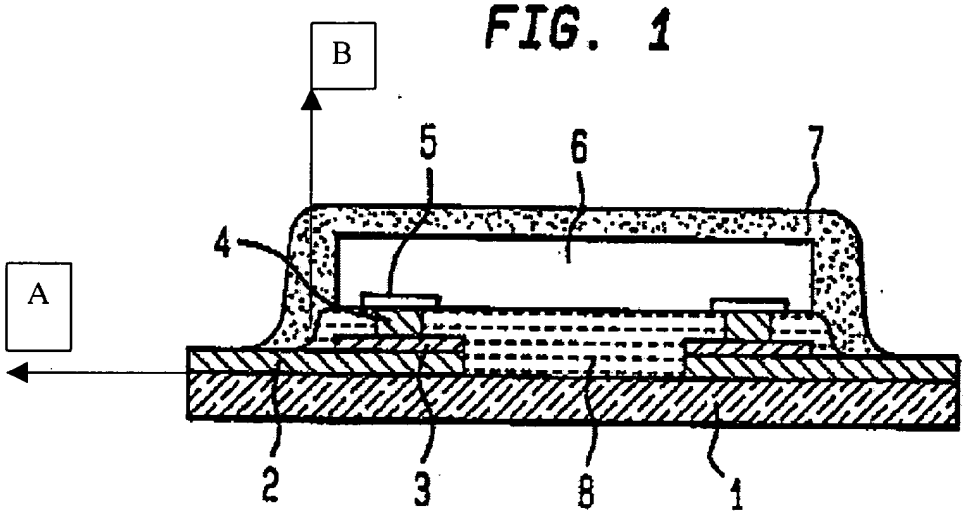
Regarding claim 21, Shin et al. discloses in Fig. 1A, Fig. 1B, Fig. 10B, Fig. 14 and column 6, lines 36 ~ 40 a semiconductor package device, comprising:

- an insulative housing (40) with a top surface, a bottom surface, and peripheral side surfaces between the top and bottom surfaces;
- a semiconductor chip (20) within and surrounded by the insulative housing, wherein the chip includes an upper surface and a lower surface, and the upper surface includes a conductive pad;
- a terminal (4 and 4') that protrudes downwardly from and extends through a central portion of the bottom surface and is spaced from the side surfaces and is electrically connected to the pad; and
- a lead (2) that protrudes laterally from and extends through one of the side surfaces and is electrically connected to the pad,
- wherein the terminal and the lead are spaced and separated from one another outside the insulative housing, and the terminal and the lead are electrically connected to one another inside the insulative housing and outside the chip.

Shin et al. does not disclose the bottom surface including a peripheral portion adjacent to the side surfaces and a central portion within the peripheral portion and spaced from the side surfaces, and the peripheral portion protrudes downwardly from the central portion. However, Nakamura et al. discloses in Fig. 1 a bottom surface (A) including a peripheral portion (B) adjacent to side surfaces and a central portion (area of 8) within the peripheral portion and spaced from the side surfaces, and the peripheral portion protruding downwardly from the central portion. Thus, it would have been obvious to one of ordinary skill in the art at the time when the invention was made to modify Shin et al. by using the peripheral portion as taught by Nakamura et al. The ordinary artisan would have been motivated to modify Shin et al. in the manner

described above for at least the purpose of providing a firm electrical connection with a circuit conductor layer formed on a substrate in a semiconductor device (column 5, lines 55 ~ 57).

FIG. 1



Regarding claims 22 and 32, Shin et al. discloses the claimed invention except for the insulative housing consisting of a first single-piece housing portion that contacts the lower surface and the lead and is spaced from the terminal and a second single-piece housing portion that contacts the first single-piece housing portion and the terminal. However, Nakamura et al. discloses in Fig. 1 an insulative housing (7 and 8) consisting of a first single-piece housing portion (7) that contacts the lower surface and the lead (2) and is spaced from the terminal (4) and a second single-piece housing portion (8) that contacts the first single-piece housing portion and the terminal. Thus, it would have been obvious to one of ordinary skill in the art at the time when the invention was made to further modify Shin et al. by using the first and second single-piece housing portion for the insulative housing as taught by Nakamura et al. The ordinary

artisan would have been motivated to further modify Shin et al. in the manner described above for at least the purpose of providing a firm electrical connection with a circuit conductor layer formed on a substrate in a semiconductor device (column 5, lines 55 ~ 57).

Regarding claims 23 and 33, Nakamura et al. discloses in Fig. 1 and Fig. 4 the first single-piece housing portion providing the top surface, the side surfaces and the peripheral portion of the bottom surface, and the second single-piece housing portion providing the central portion of the bottom surface.

Regarding claims 24 and 34, Nakamura et al. discloses in Fig. 1 the peripheral portion of the bottom surface being outside a periphery of the chip, and the central portion of the bottom surface being within and outside the periphery of the chip.

Regarding claims 25 and 35, Nakamura et al. discloses in Fig. 1, column 6, lines 49 ~ 55 and column 8, lines 53 ~ 58 the first single-piece housing portion being a transfer molded material, and the second single-piece housing portion being not a transfer molded material. Further, the limitation "transfer molded material" is a product-by-process claim language. Even though product-by-process claim is limited by and defined by the process, determination of patentability is based upon the product itself. The patentability of a product does not depend on its method of production. If the product in product-by-process claim is the same as or obvious from a product of the prior art, the claim is unpatentable even though the prior product is made by a different process. In re Thorpe, 227 USPQ 964, 966 (Fed. Cir. 1985) (citations omitted). A "product by process" claim is directed to the product per se, no matter how actually made, In re Hirao, **190 USPQ 15 at 17** (footnote 3). See also In re Brown, **173 USPQ 685**: In re Luck, **177 USPQ 523**; In re Fessmann, **180 USPQ 324**: In re Avery, **186 USPQ 116**; In re Wertheim, **191**

USPQ 90 (209 USPQ 254 does not deal with this issue); and In re Marosi et al., **218 USPQ 289** final product per se which must be determined in a "product by, all of" claim, and not the patentability of the process, and that an old or obvious product, whether claimed in "product by process" claims or not. Note that Applicant has the burden of proof in such cases, as the above caselaw makes clear.

Regarding claim 26, Nakamura et al. discloses in Fig. 1 the peripheral portion of the bottom surface protruding a first distance below the central portion of the bottom surface, the terminal protruding a second distance below the central portion of the bottom surface, and the first distance being greater than the second distance.

Regarding claim 27, Nakamura et al. discloses in Fig. 1 and Fig. 4 the peripheral portion of the bottom surface being shaped as a rectangular peripheral ledge.

Regarding claim 28, Shin et al. discloses in Fig. 1A, Fig. 1B and Fig. 10B the terminal being within a periphery of the chip, and the lead being outside the periphery of the chip.

Regarding claim 29, Shin et al. discloses in Fig. 1A, Fig. 10B and Fig. 14 the device including a plurality of terminals and leads, the chip including a plurality of pads, each of the terminals are electrically connected to one of the leads and one of the pads inside the insulative housing and outside the chip, the terminals are arranged as an array that protrudes downwardly from and extends through the bottom surface, and the leads are arranged as TSOP leads that protrude laterally from and extend through the side surface and an opposing peripheral side surface of the insulative housing.

Regarding claims 30 and 40, Shin et al. discloses in Fig. 1A, Fig. 1B and Fig. 10B the device being devoid of wire bonds, TAB leads and solder joints.

Regarding claim 31, Shin et al. discloses in Fig. 1A, Fig. 1B, Fig. 10B, Fig. 14 and column 6, lines 36 ~ 40 a semiconductor package device, comprising:

- an insulative housing (40) with a top surface, a bottom surface, and four peripheral side surfaces between the top and bottom surfaces;
- a semiconductor chip (20) within and surrounded by the insulative housing, wherein the chip includes an upper surface and a lower surface, and the upper surface includes a conductive pad, the upper surfaces faces towards the bottom surface and faces away from the top surface, and the insulative housing contacts the lower surface;
- a terminal (4 and 4') that protrudes downwardly from and extends through a central portion of the bottom surface and is spaced from the side surfaces and is electrically connected to the pad; and
- a lead (2) that protrudes laterally from and extends through one of the side surfaces and is electrically connected to the pad,
- wherein the terminal and the lead are spaced and separated from one another outside the insulative housing, and the terminal and the lead are electrically connected to one another inside the insulative housing and outside the chip.

Shin et al. does not disclose the bottom surface including a peripheral portion shaped as a rectangular peripheral ledge adjacent to the side surfaces and a recessed central portion within the peripheral portion and spaced from the side surfaces, and the peripheral portion protrudes downwardly from the central portion and extends a first distance below the central portion and wherein the terminal extends a second distance below the central portion, and the first distance is greater than the second distance. However, Nakamura et al. discloses in Fig. 1 and Fig. 4 a

bottom surface (A) including a peripheral portion (B) shaped as a rectangular peripheral ledge adjacent to the side surfaces and a recessed central portion (area of 8) within the peripheral portion and spaced from the side surfaces, and the peripheral portion protrudes downwardly from the central portion and extends a first distance below the central portion and wherein a terminal (4) extends a second distance below the central portion, and the first distance is greater than the second distance. Thus, it would have been obvious to one of ordinary skill in the art at the time when the invention was made to modify Shin et al. by using the peripheral portion as taught by Nakamura et al. The ordinary artisan would have been motivated to modify Shin et al. in the manner described above for at least the purpose of providing a firm electrical connection with a circuit conductor layer formed on a substrate in a semiconductor device (column 5, lines 55 ~ 57).

Regarding claim 36, Nakamura et al. discloses in Fig. 1 the first distance being about twice the second distance.

Regarding claim 37, Nakamura et al. discloses in Fig. 1 the peripheral portion of the bottom surface being integral with the side surfaces and non-integral with the central portion of the bottom surface.

Regarding claim 38, Shin et al. discloses in Fig. 10B the terminal being within a periphery of the chip, and the peripheral portion of the bottom surface is outside the periphery of the chip.

Regarding claim 39, Shin et al. discloses in Fig. 1A, Fig. 10B and Fig. 14 the device including a plurality of terminals and leads, the chip including a plurality of pads, each of the terminals being electrically connected to one of the leads and one of the pads inside the

insulative housing and outside the chip, the terminals are arranged as an array that protrudes downwardly from and extends through the central portion of the bottom surface, and the leads are arranged as TSOP leads that protrude laterally from and extend through two of the side surfaces that oppose one another.

9. Claims 41, 45 ~ 51 and 57 ~ 60 are rejected under 35 U.S.C. 103(a) as being unpatentable over Shin et al. in view of Kuraishi et al.

Regarding claim 41, Shin et al. discloses in Fig. 1A, Fig. 1B, Fig. 10B, Fig. 14 and column 6, lines 36 ~ 40 a semiconductor package device, comprising:

- an insulative housing (40) with a top surface, a bottom surface, and a peripheral side surface between the top and bottom surfaces;
- a semiconductor chip (20) within the insulative housing, wherein the chip includes an upper surface and a lower surface, and the upper surface includes a conductive pad;
- a terminal (4) that protrudes downwardly from and extends through the bottom surface and is electrically connected to the pad; and
- a lead (2) that protrudes laterally from and extends through the side surface and is electrically connected to the pad,
- wherein the terminal and the lead are spaced and separated from one another outside the insulative housing, and the terminal and the lead are electrically connected to one another inside the insulative housing and outside the chip.

Shin et al. does not disclose the lead includes a recessed portion. However, Kuraishi et al. discloses in Fig. 4 the lead including a recessed portion (upper part of 18) that extends through a

side surface and is spaced from top and bottom surfaces and a non-recessed portion (20) that extends outside an insulative housing (26) and is adjacent to the recessed portion. Thus, it would have been obvious to one of ordinary skill in the art at the time when the invention was made to modify Shin et al. by using the peripheral portion as taught by Kuraishi et al. The ordinary artisan would have been motivated to modify Shin et al. in the manner described above for at least the purpose of providing a semiconductor device that can easily be mounted on a printed circuit board (column 2, lines 3 and 4).

A further difference between Shin et al., as modified, and claimed invention is a non-recessed portion of a lead being located at a corner between a side surface and a bottom surface. However, such a difference is regard as nothing more than obvious design variation of Shin et al. Therefore, it would have been obvious to one having ordinary skill in the art at the time the invention was made to have the non-recessed portion of the lead at the location of a "corner between a side surface and a bottom surface." The ordinary artisan would have been motivated to further modify Shin et al. in the manner described above for at least the purpose of decreasing manufacture cost by decreasing number of lead bending.

Regarding claim 45, Shin et al. discloses in Fig. 1A, Fig. 1B and Fig. 10B the terminal being the only electrical conductor that extends through the top or bottom surfaces and being electrically connected to the pad.

Regarding claim 46, Shin et al. discloses in Fig. 1A, Fig. 1B and Fig. 10B the terminal being a plated metal. Further, the limitation "plated metal" is a product-by-process claim language. Even though product-by-process claim is limited by and defined by the process, determination of patentability is based upon the product itself. The patentability of a product

does not depend on its method of production. If the product in product-by-process claim is the same as or obvious from a product of the prior art, the claim is unpatentable even though the prior product is made by a different process. In re Thorpe, 227 USPQ 964, 966 (Fed. Cir. 1985) (citations omitted). A "product by process" claim is directed to the product per se, no matter how actually made, In re Hirao, **190 USPQ 15 at 17** (footnote 3). See also In re Brown, **173 USPQ 685**: In re Luck, **177 USPQ 523**; In re Fessmann, **180 USPQ 324**: In re Avery, **186 USPQ 116**; In re Wertheim, **191 USPQ 90 (209 USPQ 254** does not deal with this issue); and In re Marosi et al., **218 USPQ 289** final product per se which must be determined in a "product by, all of" claim, and not the patentability of the process, and that an old or obvious product, whether claimed in "product by process" claims or not. Note that Applicant has the burden of proof in such cases, as the above caselaw makes clear.

Regarding claim 47, Shin et al. discloses in Fig. 1A, Fig. 1B and Fig. 10B the terminal being within a periphery of the chip, and the lead being outside the periphery of the chip.

Regarding claim 48, Shin et al. discloses in Fig. 1A, Fig. 1B and Fig. 10B the device is devoid of an electrical conductor that extends through the top surface and is electrically connected to the pad.

Regarding claim 49, Shin et al. discloses in Fig. 1A, Fig. 10B and Fig. 14 the device including a plurality of terminals and leads, the chip including a plurality of pads, each of the terminals being electrically connected to one of the leads and one of the pads inside the insulative housing and outside the chip, the terminals are arranged as an array that protrudes downwardly from and extends through the bottom surface, and the leads are arranged as TSOP

leads that protrude laterally from and extend through the side surface and an opposing peripheral side surface of the insulative housing.

Regarding claims 50 and 60, Shin et al. discloses in Fig. 1A, Fig. 1B and Fig. 10B the device being devoid of wire bonds, TAB leads and solder joints.

Regarding claim 51, Shin et al. discloses in Fig. 1A, Fig. 1B, Fig. 10B, Fig. 14 and column 6, lines 36 ~ 40 A semiconductor package device, comprising:

- an insulative housing (40) with a top surface, a bottom surface, and a peripheral side surface between the top and bottom surfaces;
- a semiconductor chip (20) within and surrounded by the insulative housing, wherein the chip includes an upper surface and a lower surface, the upper surface includes a conductive pad (31), the upper surfaces faces towards the bottom surface and faces away from the top surface, and the insulative housing contacts the lower surface;
- a terminal (4 and 4') that protrudes downwardly from and extends through the bottom surface and is spaced from the side surface and is electrically connected to the pad; and
- a lead (2) that protrudes laterally from and extends through the side surface and is electrically connected to the pad,
- wherein the terminal and the lead are spaced and separated from one another outside the insulative housing, and the terminal and the lead are electrically connected to one another inside the insulative housing and outside the chip.

Shin et al. does not disclose the lead includes a recessed portion. However, Kuraishi et al. discloses in Fig. 4 the lead including a recessed portion (upper part of 18) inside an insulative

housing that extends through a side surface and is spaced from top and bottom surfaces and a non-recessed portion (20) outside an insulative housing (26) that is adjacent to and integral with the recessed portion and contacts the side surface. Thus, it would have been obvious to one of ordinary skill in the art at the time when the invention was made to modify Shin et al. by using the peripheral portion as taught by Kuraishi et al. The ordinary artisan would have been motivated to modify Shin et al. in the manner described above for at least the purpose of providing a semiconductor device that can easily be mounted on a printed circuit board (column 2, lines 3 and 4).

A further difference between Shin et al., as modified, and claimed invention is a non-recessed portion of a lead being adjacent to a corner between a side surface and a bottom surface. However, such a difference is regard as nothing more than obvious design variation of Shin et al. Therefore, it would have been obvious to one having ordinary skill in the art at the time the invention was made to have the non-recessed portion of the lead at the location of a "corner between a side surface and a bottom surface." The ordinary artisan would have been motivated to further modify Shin et al. in the manner described above for at least the purpose of decreasing manufacture cost by decreasing number of lead bending.

Regarding claim 57, Shin et al. discloses in Fig. 1A, Fig. 1B and Fig. 10B the terminal being within a periphery of the chip and outside a periphery of the pad, and the lead being outside the periphery of the chip.

Regarding claim 58, Shin et al. discloses in Fig. 10B and column 21, lines 22 ~ 28 the terminal being integral with a routing line that is plated on the lead inside the insulative housing, outside a periphery of the terminal and outside a periphery of the chip. Further, the limitation

"plated on the lead" is a product-by-process claim language. Even though product-by-process claim is limited by and defined by the process, determination of patentability is based upon the product itself. The patentability of a product does not depend on its method of production. If the product in product-by-process claim is the same as or obvious from a product of the prior art, the claim is unpatentable even though the prior product is made by a different process. In re Thorpe, 227 USPQ 964, 966 (Fed. Cir. 1985) (citations omitted). A "product by process" claim is directed to the product per se, no matter how actually made, In re Hirao, **190 USPQ 15 at 17** (footnote 3). See also In re Brown, **173 USPQ 685**: In re Luck, **177 USPQ 523**; In re Fessmann, **180 USPQ 324**: In re Avery, **186 USPQ 116**; In re Wertheim, **191 USPQ 90 (209 USPQ 254** does not deal with this issue); and In re Marosi et al., **218 USPQ 289** final product per se which must be determined in a "product by, all of" claim, and not the patentability of the process, and that an old or obvious product, whether claimed in "product by process" claims or not. Note that Applicant has the burden of proof in such cases, as the above caselaw makes clear.

Regarding claim 59, Shin et al. discloses in Fig. 1A, Fig. 1B and Fig. 10B the device including a plurality of terminals and leads, the chip including a plurality of pads, each of the terminals being electrically connected to one of the leads and one of the pads inside the insulative housing and outside the chip, the terminals are arranged as an array that protrudes downwardly from and extends through the bottom surface, and the leads are arranged as TSOP leads that protrude laterally from and extend through the side surface and an opposing peripheral side surface of the insulative housing.

10. Claims 42 ~ 44 and 52 ~ 56 are rejected under 35 U.S.C. 103(a) as being unpatentable over Shin et al. and Kuraishi et al. as applied to claim 41 above, and further in view of Nakamura et al.

Regarding claim 42, Shin et al., as modified, discloses the claimed invention except for the insulative housing including a first single-piece housing portion that contacts the lead and is spaced from the terminal and a second single-piece housing portion that contacts the first single-piece housing portion and the terminal. However, Nakamura et al. discloses in Fig. 1 an insulative housing (7 and 8) including a first single-piece housing portion (7) that contacts a lead (2) and is spaced from a terminal (4) and a second single-piece housing portion (8) that contacts the first single-piece housing portion and the terminal. Thus, it would have been obvious to one of ordinary skill in the art at the time when the invention was made to modify Shin et al. by using the first and second single-piece housing portion for the insulative housing as taught by Nakamura et al. The ordinary artisan would have been motivated to modify Shin et al. in the manner described above for at least the purpose of providing a firm electrical connection with a circuit conductor layer formed on a substrate in a semiconductor device (column 5, lines 55 ~ 57).

Regarding claim 43, Nakamura et al. discloses in Fig. 1 the first single-piece housing portion contacting the lower surface.

Regarding claim 44, Nakamura et al. discloses in Fig. 1 the insulative housing consisting of the first and second single-piece housing portions.

Regarding claim 52, Shin et al., as modified, discloses the claimed invention except for the insulative housing consists of a first single-piece housing portion that contacts the lower

surface and the lead and is spaced from the terminal and a second single-piece housing portion that contacts the first single-piece housing portion and the terminal. However, Nakamura et al. discloses in Fig. 1 an insulative housing (7 and 8) consisting of a first single-piece housing portion (7) that contacts a lower surface and a lead (2) and is spaced from a terminal (4) and a second single-piece housing portion (8) that contacts the first single-piece housing portion and the terminal. Thus, it would have been obvious to one of ordinary skill in the art at the time when the invention was made to modify Shin et al. by using the first and second single-piece housing portion for the insulative housing as taught by Nakamura et al. The ordinary artisan would have been motivated to modify Shin et al. in the manner described above for at least the purpose of providing a firm electrical connection with a circuit conductor layer formed on a substrate in a semiconductor device (column 5, lines 55 ~ 57).

Regarding claim 53, Nakamura et al. discloses in Fig. 1 the first single-piece housing portion providing the top surface, the side surface and a peripheral portion of the bottom surface, and the second single-piece housing portion providing a central portion of the bottom surface within the peripheral portion of the bottom surface.

Regarding claim 54, Nakamura et al. discloses in Fig. 1 the peripheral portion of the bottom surface being outside a periphery of the chip, and the central portion of the bottom surface being within and outside the periphery of the chip.

Regarding claim 55, Nakamura et al. discloses in Fig. 1 the first single-piece housing portion being a transfer molded material, and the second single-piece housing portion being not a transfer molded material. Further, the limitation "transfer molded material" is a product-by-process claim language. Even though product-by-process claim is limited by and defined by the

process, determination of patentability is based upon the product itself. The patentability of a product does not depend on its method of production. If the product in product-by-process claim is the same as or obvious from a product of the prior art, the claim is unpatentable even though the prior product is made by a different process. In re Thorpe, 227 USPQ 964, 966 (Fed. Cir. 1985) (citations omitted). A "product by process" claim is directed to the product per se, no matter how actually made, In re Hirao, **190 USPQ 15 at 17** (footnote 3). See also In re Brown, **173 USPQ 685**: In re Luck, **177 USPQ 523**; In re Fessmann, **180 USPQ 324**: In re Avery, **186 USPQ 116**; In re Wertheim, **191 USPQ 90 (209 USPQ 254** does not deal with this issue); and In re Marosi et al., **218 USPQ 289** final product per se which must be determined in a "product by, all of" claim, and not the patentability of the process, and that an old or obvious product, whether claimed in "product by process" claims or not. Note that Applicant has the burden of proof in such cases, as the above caselaw makes clear.

Regarding claim 56, Nakamura et al. discloses in Fig. 1 the second single-piece housing portion including first and second opposing surfaces, the first surface contacting the lead and the second surface providing a portion of the bottom surface.

Conclusion

11. The prior art made of record and not relied upon is considered pertinent to applicant's disclosure.

Nakaya et al. discloses in column 6, lines 11 ~ 12 a silicon film is non-transparent.

Distefano et al. (U.S. Pat. No. 6,468,836), Glenn et al., Bai et al., Lee, Hong et al., Distefano et al. (U.S. Pat. No. 6,232,152), Smith et al., Akram et al., Kweon et al., Lee et al., King et al., Park et al., Takahashi et al., McShane et al., Endoh et al., Hodge, Bruner, Happ and Hirata disclose a semiconductor device.

Any inquiry concerning this communication or earlier communications from the examiner should be directed to Chris C. Chu whose telephone number is (703) 305-6194. The examiner can normally be reached on M-F (10:30 - 7:00).

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Eddie C. Lee can be reached on (703) 308-1690. The fax phone numbers for the organization where this application or proceeding is assigned are (703) 308-7382 for regular communications and (703) 308-7722 for After Final communications.

Any inquiry of a general nature or relating to the status of this application or proceeding should be directed to the receptionist whose telephone number is (703) 308-0956.

Chris C. Chu
Examiner
Art Unit 2815

c.c.
April 17, 2003

SHEILA V. CLARK
PRIMARY EXAMINER